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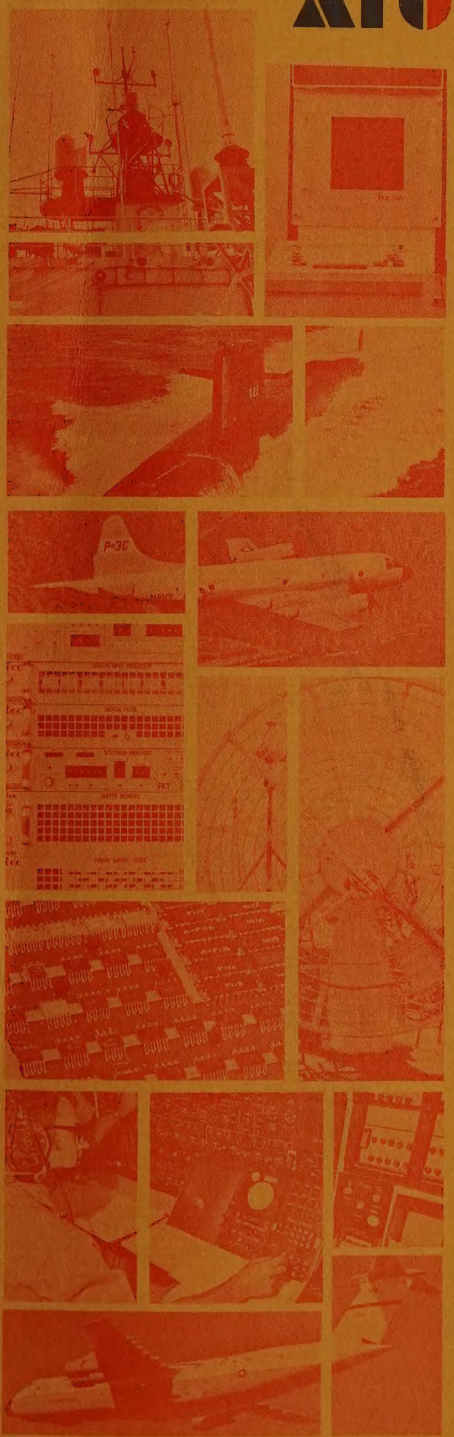

PDA-142 PLASMA DISPLAY HEAD

USER MANUAL

MP MASTER

MA28303

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USER MANUAL

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1.0 INTRODUCTION

This bulletin provides general information useful to the system designer in understanding the operation of characteristics of the PDA 142 Plasma Display Unit.

The PDA 142 is a digitally addressed graphic display which uses a 512 x 512 dot matrix, AC plasma panel as its display medium. Information is formed by dots of light (gas discharges) which can be randomly written or erased without disturbing any other information already displayed. It is also possible to erase all gas discharges in one operation (BULK ERASE).

The process of writing and erasing dots is called ADDRESSING. Dots can be addressed either one at a time (SERIAL mode) or in groups of up to 16 (PARALLEL mode) during each address operation. This choice of mode allows the use of the most efficient addressing method to display a given type of information. The SERIAL MODE is best for most types of graphics and for vector generation. The PARALLEL MODE lends itself to high speed text editing applications as well as to displaying "buffer-loaded" graphics.

Once information has been displayed, it will remain without any external influence from support hardware so long as power to the display is not interrupted. This ability to maintain information is referred to as INHERENT MEMORY, and makes refreshing unnecessary. Addresses pertinent to the displayed information do not have to be stored except as may be necessary to process data. (Information may not be retrieved electronically from the display unit.)

2.0 GENERAL

2.1 Typical Characteristics

Physical:	
Dot matrix size	512 x 512
Resolution	60 Dots per inch (24 dots per cm)
Dot spacing	16.7 mils (.42mm) center to center
Display size (active area)	8.5" x 8.5" (21.7 cm x 21.7 cm)
Character capacity:[1]	
5 x 7 (6 x 10) Matrix	4335 Characters
	51 Lines
	85 Characters per line
7 x 9 (8 x 16) Matrix	2048 Characters
	32 Lines
	64 Characters per line
Dot brightness	60 footlamberts
Contrast ratio	25:1
Dot size	9 mils (.23 mm)
Viewing angle	160°
Color	Neon orange (5852 Å predominant)
Electrical:	
Data interface:	
Input	9 X Address lines
	9 Y Address lines
	16 Y Parallel Address lines
	Serial/Parallel mode select line
	2 Control lines (select WRITE, ERASE, and BULK ERASE operations)
Output	SYNC (50KHz clock)
	STATUS (Busy/Done indicator)
Type interface	TTL with resistor pull up to V_{CC}
Operational rates:	
Maximum address rate	800K dots per second
Vector rate (serial)	50K dots per second
Character rate (serial)	833 characters per second [5x7 (6x10) Matrix]
	390 characters per second [7x9 (8x16) Matrix]
Character rate (parallel)	8333 characters per second [5x7 (6x10) Matrix
	6250 characters per second [7x9 (8x16) Matrix
Full panel bulk erase	20 microseconds
Automatic bulk erase	30 minutes after last address operation
Data modes	Asynchronous or synchronous
Mechanical:	
Size	See figure 2.1
Weight	34 pounds (15.4 Kg)

1-Display is non-formatted, character matrix sizes are given for information only.

Environmental:

Temperature range:	
Operational	0°C to +50°C (0°C to +35°C)[2]
Storage	-40°C to +70°C (-40°C to +50°C)[2]
Humidity	10-80% noncondensing/noncorrosive[3]

2-Parenthesized ranges refer to display with contrast enhancing filter and rear projection screen installed.
3-Without contrast enhancing filter and rear projection screen installed.

2.2 Mechanical Dimensions

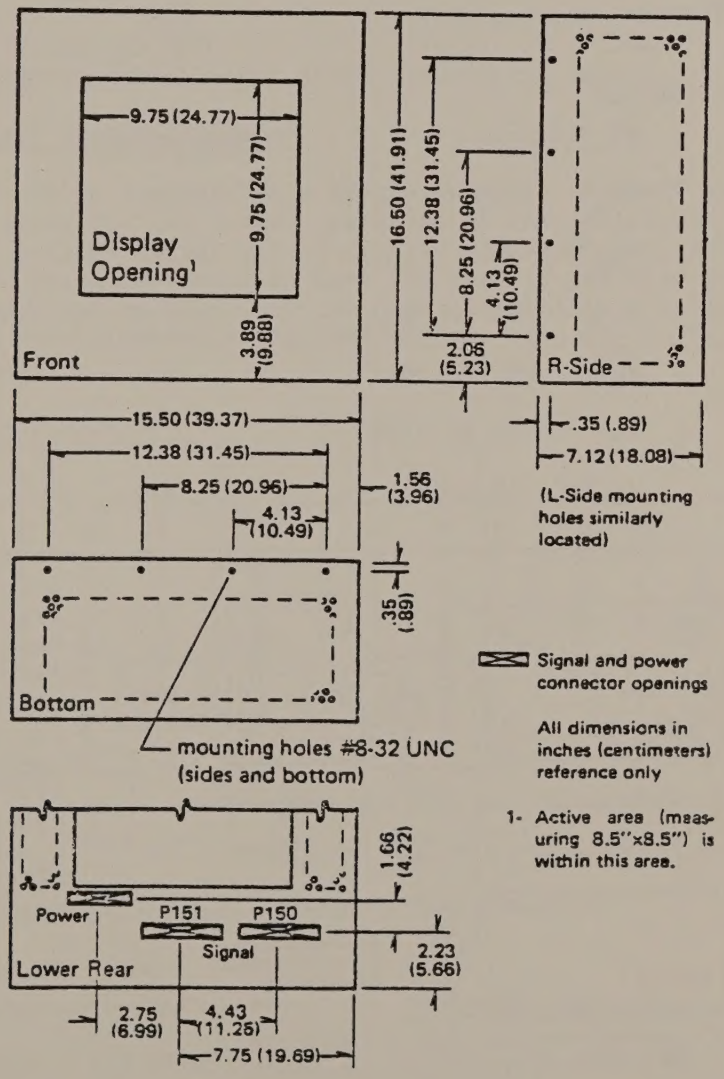


Figure 2.1 - Display Dimensions

2.3 Power Supply

Mechanical:

Size	See figure 2.2
Weight	23.5 pounds (10.5 Kg)

Environmental:

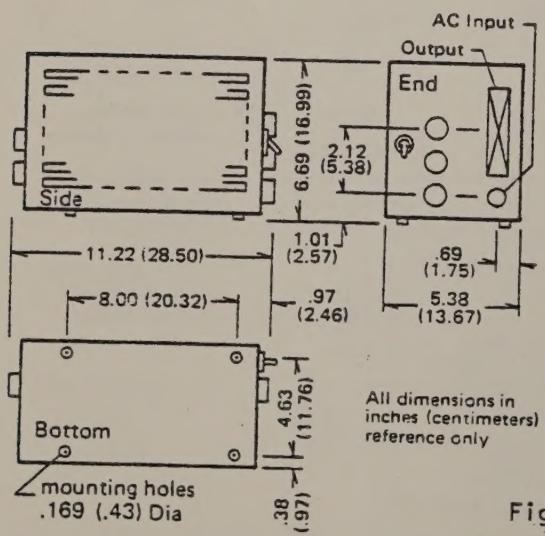
Temperature range:	
Operational	0°C to +50°C
Storage	-40°C to +70°C
Humidity	10-80% noncondensing/noncorrosive

Power:

Input	105-125 VAC 50/60Hz 2.5 amperes 210-240 VAC 50/60Hz 1.25 amperes

Output

DC Voltages		Amperes (max)	Total Regulation[1]
V_{CC}[2]	+4.8 to +5.25	3.75	.7%
V_{SC}[5]	+9 ±1	2.0	30%
V_{AX}	+65 to +85	.175	.5%
V_{AY}	-65 to -85	.175	.5%
V_{SS}	+85 to +105	.73	.5%
V_{SB}[4,5]	+38 ±10	.050	10%



1-Includes the effects of line, load, and temperature variations.
2-Remote sensing provided.
3-For intermittent periods of less than 5 minutes.
4-For approximately 20 seconds after AC power is first applied, V_{SB} boosts to a level within a range of +100 to +130 volts DC.
5-Nonadjustable.

Figure 2.2 - Mechanical Dimensions

2.4 Protection

The power pack is protected against overcurrent conditions by the following means:

Input: 105-125VAC 4A Slo-Blo line fuse
210-240VAC 2A Slo-Blo line fuse

Output	Supply	Type
	V_{CC}	5A Fuse/Current limiting
	V_{SC}	3A Fuse
	V_{AX}	.25A Fuse/Current limiting
	V_{AY}	.25A Fuse/Current limiting
	V_{SS}	.6A Fuse/Current limiting
	V_{SB}	.375A and .6A (boost circuit) fuses

Power transformer thermal cutout (automatic reset)

2.5 Power Pack and Display Pairing

A power pack which accompanies a display unit in shipment has been preadjusted for the proper operation of that display. (The serial numbers of the paired display and power pack are noted on the system information card attached to the display.) The power pack can be used with any other compatible display; however, it may be necessary to readjust the V_{SS}, V_{AX}, or V_{AY} voltage level

2.6 Power Output Connector

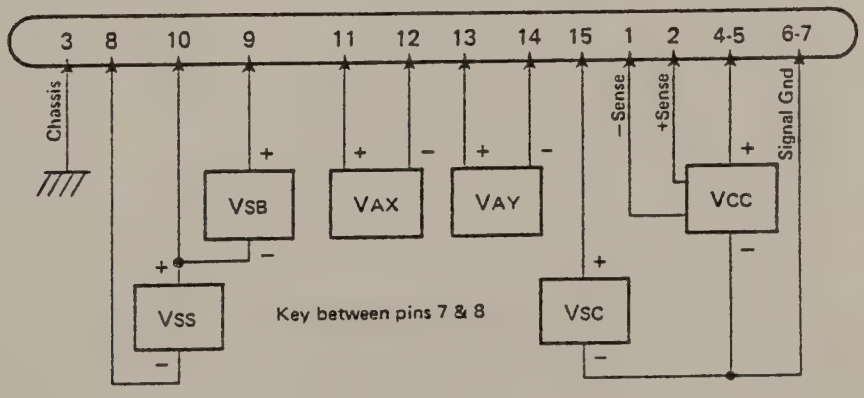


Figure 2.3 - Power Output Connector

Mating connector type:

Manufacturer — AMP

Part	Qty	MFG. Part No.
Housing	1	583301-1
Contacts	15	583362-4
Key	1	583462-1

2.7 Rear Projection

This display has several unique characteristics that allow the projection of images onto the rear of the display panel. Using this capability, photographic images of forms, maps, or any other projectionable material may be integrated with displayed information.

A frosted projection screen is provided on the rear surface of the plasma panel. Figure 2.2 illustrates its position in relation to the plane of the gas discharges. When using the rear projection capability, consideration should be given to the parallax resulting from the separation of the planes of the gas discharge and the projected image.

If the rear projection capability is not to be used, it is suggested that a piece of black paper be placed over the rear of the projection screen to shut out ambient light and insure maximum display contrast.

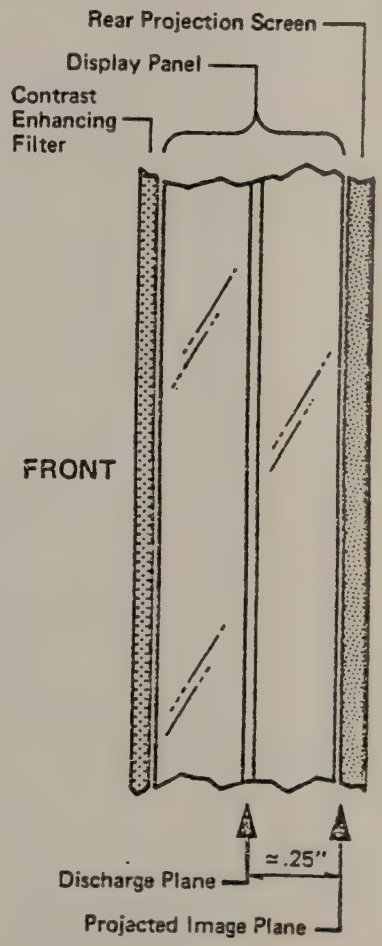


Figure 2.4 - Cross Sectional View of Panel Assembly

2.8 Display Origin

The display origin (0,0 coordinate) is located in the lower left corner of the display matrix. It can, if necessary, be relocated to the upper left corner.

2.9 Cleaning the Display Panel

Avoid allowing any object, particularly fingers, to contact the surface of the polarizing filter and rear projection screen installed on the display panel. These surfaces can be permanently marred and their usefulness impaired through careless use or improper cleaning.

To clean the polarizing filter and rear projection screen, first lightly dust them with a soft cloth or tissue to

remove loose soil. Then, using only a mild detergent and water solution on a soft cloth or tissue, gently wipe the surfaces until they are clean. If the surfaces are soiled by a dried or gritty material, carefully moisten the soiled areas until the material is dissolved or loosened before wiping it away. Dry the surfaces with a soft cloth or tissue. Never scrub the surfaces or use cleaning solvents.

The display enclosure may be cleaned using a soft cloth slightly moistened with a mild detergent and water solution. Do not allow the cleaning solution to get inside the enclosure.

3.0 INTERFACE SIGNALS

3.1 Interface Signal Levels and Conventions

The positive logic convention is used to describe interface signal levels for the display. HI indicates the more positive voltage level; the logical "1" or "true" state. LO indicates the more negative voltage level (at or near system ground); the logical "0" or "false" state.

The following signal voltage specifications are as measured at the interface connector on the display unit:

LO input	=	+0.8 VDC maximum
HI input	=	+2.0 VDC minimum
LO output	=	+0.8 VDC maximum
HI output	=	+2.4 VDC minimum

Each interface input signal is buffered inside the display by a 7400 series TTL logic element which represents one standard TTL unit load. Each input signal is also terminated by a 1000 ohm resistor to +5VDC (Vcc). Input signals that are not connected will be held HI by this termination resistor.

Each interface output signal as it appears at the interface connector represents and is capable of driving one standard TTL unit load.

3.2 Address Signal Inputs

The matrix locations of the dots to be addressed are specified by the ADDRESS SIGNALS. These signals are divided into three groups called the X ADDRESS, Y ADDRESS, and Y PARALLEL ADDRESS signals.

3.2.1 Serial Mode

When using the display in the serial mode, only the X Address and Y Address signals are required to address a single dot anywhere within the display matrix (see figure 3.1, page 8). These signals are used to select one of the 512 electrodes (numbered 0 through 511) in both the X and the Y axis. The dot located at the intersection of the selected electrodes will be the only one addressed; the on or off state of all others in the active area will remain unchanged.

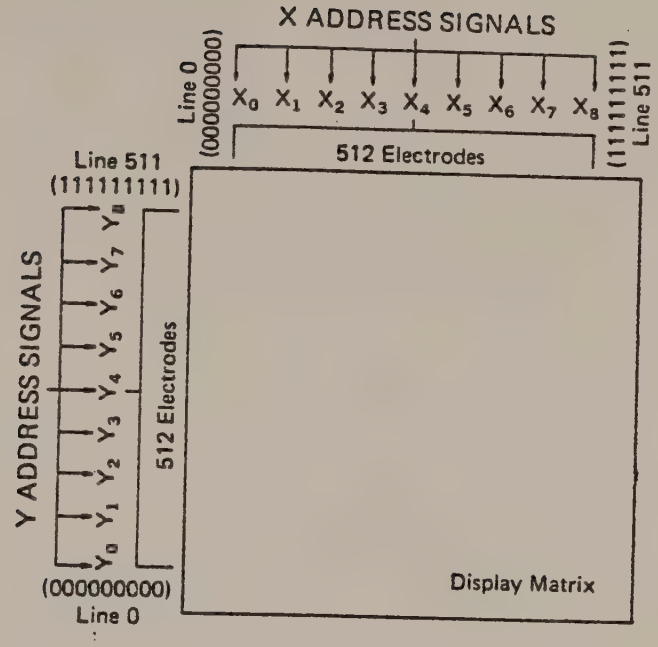


Figure 3.1 - Address Signals in Serial Mode

The X Address and Y Address signals comprise two nine bit binary words, each consisting of bit 0 having a binary value of 1, through bit 8 with a value of 256. The binary values of these words represent the numbers of the intersecting electrodes or coordinates for the desired dot. (If all X and Y Address signals are LO, the selected dot will be located at the display origin or 0,0 coordinate.)

3.2.2 Parallel Mode

Parallel operation requires the use of the X Address and Y Parallel Address signals, and bits 3 through 8 of the Y Address signals. Rather than selecting a single dot as in serial operation, the parallel mode allows a vertical column of dots, 16 dots high, to be addressed (see figure 3.2). Any number of dots within the specified column can be written or erased without changing the on or off state of the remaining dots in the column. (Dots cannot be both written and erased during a given address operation.)

The X axis electrode that intersects the horizontal location of the desired column of dots is selected using the X Address signals. These signals select the appropriate electrode in a manner similar to that as when operating in the serial mode. To indicate the vertical location of the desired column, only

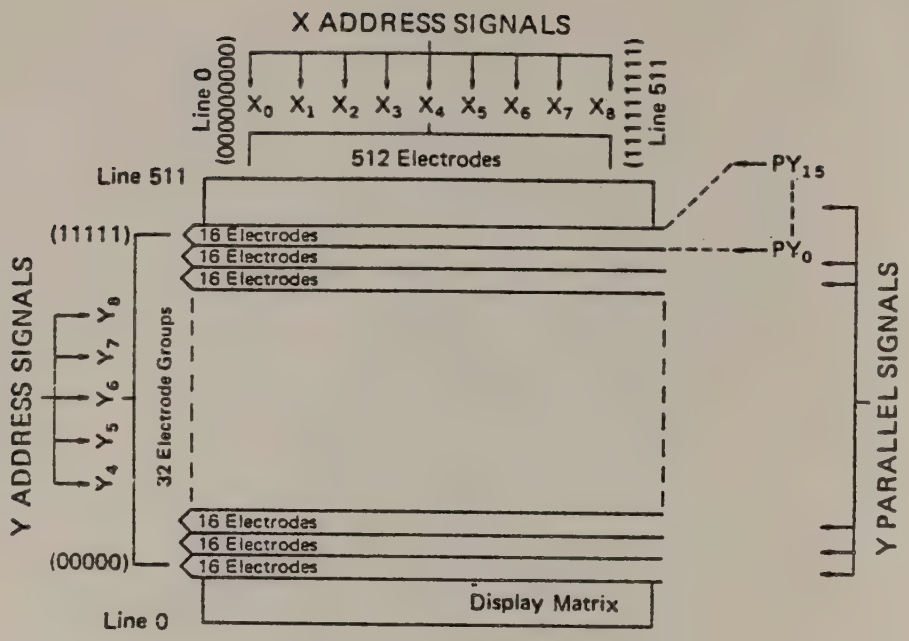


Figure 3.2 - Address Signals in Parallel Mode

bits 3 through 8 of the Y Address signals are needed. These bits locate one of the 32 horizontal bands of electrodes (called SECTORS) in the display matrix. The column of dots is located where the selected Y sector and X electrode intersect.

The actual dots within the specified column that are to be addressed are selected by the 16 Y Parallel Address signals. These are labeled PY_0 through PY_{15} and correspond, respectively, to the bottom most to top most dots in the column. By holding the appropriate PY signal LO, the corresponding dot in the column will be addressed. The on or off state of the dots corresponding to the PY signals that remain HI will not change.

3.3 Mode Select Input

Serial or parallel operation of the display is selected using the Mode Select signal. A HI level at this input will select serial operation of the display; a LO level, parallel operation.

If the Mode Select signal is not connected, the input will be held HI by the interface termination resistor (see section 3.1). In this case, the display will automatically operate in the serial mode.

3.4 Control Signal Inputs

The display WRITES or ERASES individually addressed points in the display matrix, or BULK ERASES all illuminated points simultaneously, as directed by two control input signals, C_0 and C_1. The use of these signals is illustrated in figure 3.1.

CONTROL SIGNALS C_0	C_1	DISPLAY OPERATION
1	1	Idle
1	0	Write
0	1	Erase
0	0	Bulk Erase

Figure 3.3 - Control Signals and Display Operation

CONTROL SIGNALS *WRITE*	*ERASE*	*BULK*	DISPLAY OPERATION
0	0	0	Idle
1	0	0	Write
0	1	0	Erase
0	1	1	Bulk Erase

Figure 3.4 - Alternate Control Signals and Display Operation

As a convenience in existing applications where earlier model 512-60 displays have been used, individual WRITE, ERASE, and BULK ERASE control signals have been provided. These signals serve the same function as the C_0 and C_1 signals and are used as illustrated in figure 3.2.

Either set of control signals may be used, but not simultaneously.

3.5 STATUS Signal Output

STATUS is an output signal which serves as the display busy/done indicator.

When the display is idle, with or without information being displayed, STATUS will rest in the HI state. STATUS goes LO to indicate that the display is busy executing operations as directed by the CONTROL signals.

3.6 SYNC Signal Output

SYNC is a display generated clock output which is used to synchronize external circuits with the operation of the display. SYNC is normally LO with a positive going pulse occurring every 20 microseconds (50KHz).

3.7 Interface Signal Connectors

All logic level interface signals associated with display operation are accessible through the two printed circuit edge connectors on the back of the display unit (see figure 2.1 for location). Figure 3.5 lists the pin assignments for these connectors.

The display can be used without connecting any of the P150 connector signals. In this case the display will operate in the serial mode only. This is useful in applications where the D142 display replaces a serially addressed D141 model 512-60 display.

P150

PIN#	SIGNAL	PIN#	SIGNAL
1	N/C	16	PY_6
2	N/C	17	PY_7
3	N/C	18	PY_8
4	N/C	19	PY_9
5	N/C	20	PY_{10} †
6	N/C	21	PY_{11}
7	N/C	22	PY_{12}
8	N/C	23	PY_{13}
9	Mode Sel	24	PY_{14}
10	PY_0	25	PY_{15}
11	PY_1	26	N/C
12	PY_2	27	N/C
13	PY_3	28	N/C
14	PY_4	29	N/C
15	PY_5	30	N/C

Pins A thru j - Signal Gnd

†Key

P151

PIN#	SIGNAL	PIN#	SIGNAL
1	Gnd*	16	N/C
2	+5VDC*	17	Y_1
3	SYNC	18	X_1
4	STATUS	19	X_2
5	Write	20	X_4
6	Bulk †	21	Y_8
7	Erase	22	Y_3
8	X_0	23	Y_4
9	X_3	24	Y_6
10	X_5	25	Y_7
11	X_7	26	Y_2
12	X_6	27	Y_5
13	X_8	28	Y_0
14	C_0	29	Chassis Gnd
15	C_1	30	Signal Gnd

Pins A thru J - Signal Gnd

Voltage output - 375ma (max) (see section 5.3)

†Key

Figure 3.5 - Interface Connector Wiring Lists (P150 and P151)

Mating Connector Type for P150 and P151: Manufacturer - AMP

Part	QTY	Mfg. Part No.
Housing	1	1-583718-3
Contacts	60	583854-5
Key	1	583274-1

4.0 DISPLAY OPERATION

4.1 Asynchronous Mode

The display may be addressed asynchronously by presenting the appropriate ADDRESS, CONTROL, and MODE SELECT signals simultaneously while STATUS is resting in the HI state (see figure 4.1). Within 20 microseconds after presentation of these signals, STATUS will go LO indicating that the display has begun execution of the requested operation.

The CONTROL signals may be returned to their idle state or be updated for the next operation after the HI to LO transition or STATUS.

The ADDRESS and MODE SELECT signals are not stored by the display so they must be held at their appropriate levels the entire time that STATUS is LO. After the display has completed execution of the requested operation and STATUS has returned HI, these signals may be changed.

If another operation has been requested by the CONTROL SIGNALS as STATUS returns HI, STATUS will remain HI for

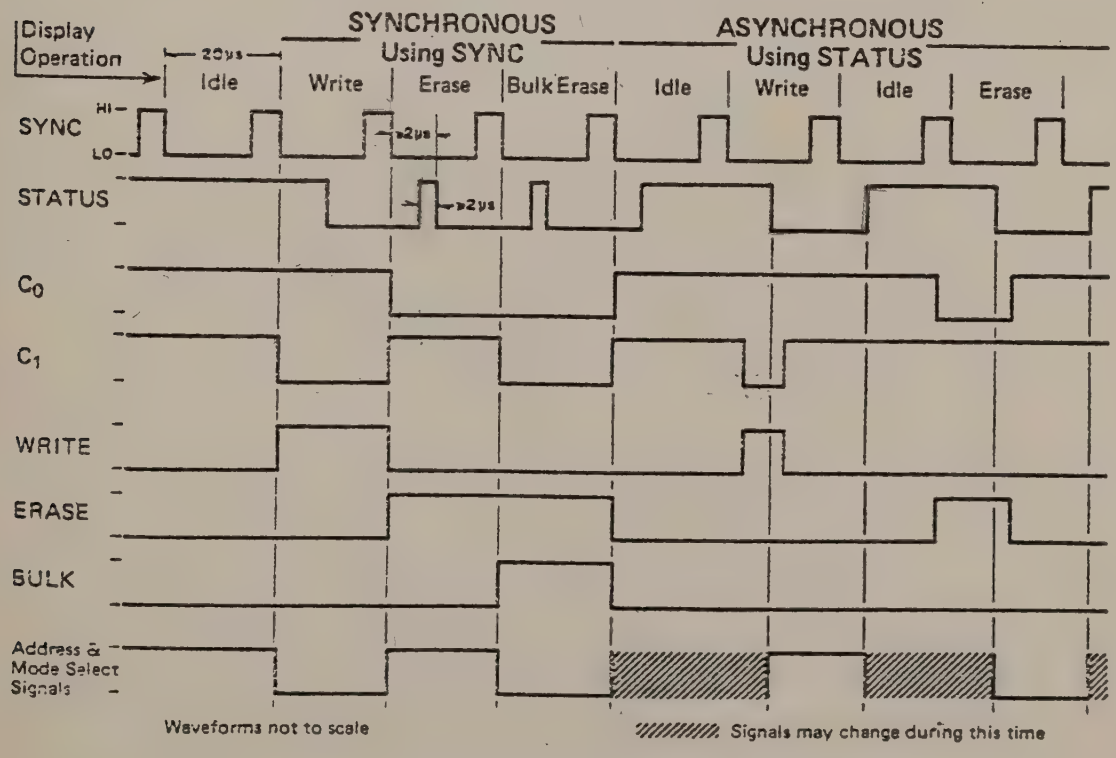


Figure 4.1 - Typical Interface Signal Waveforms

a minimum of 2 microseconds before once again going LO, to indicate that the display has begun execution of the new operation. The ADDRESS and MODE SELECT signals must be updated for the new operation while STATUS is HI.

4.2 Synchronous Mode

The display may be addressed synchronously at its maximum address rate by using the SYNC signal. This is accomplished by presenting and then subsequently updating the appropriate ADDRESS, CONTROL, and MODE SELECT signals within 2 microseconds following the HI to LO transition of SYNC (see figure 4.1). These signals should not change until the reoccurrence of the HI to LO transition of SYNC.

For added flexibility, the display may be addressed synchronously using both the SYNC and STATUS signals. In this case the ADDRESS, CONTROL, and MODE SELECT signals are presented or updated within 2 microseconds following the HI to LO transition of SYNC as described in the foregoing paragraph. However, if desired, the CONTROL signals may be changed as soon as STATUS goes LO. The ADDRESS and MODE SELECT signals must remain at their appropriate levels until the reoccurrence of the SYNC signal's HI to LO transition.

4.3 Automatic Bulk Erase

Automatic bulk erase is a display controlled operation which automatically erases the entire display screen when the display has been left idle for an extended period of time. The automatic bulk erase will be executed approximately 30 minutes after the last address operation regardless of whether information is actually being displayed, and will repeat at 30 minute intervals for as long as the display is turned on and left idle.

CAUTION

Automatic bulk erase is provided to protect the display and extend its life. Do not leave the display idle with the CONTROL signals set for a WRITE or ERASE operation as this will disable the AUTOMATIC BULK ERASE feature. (See section 4.4, Uniform Display Usage.)

NOTES

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